Timing constraint: Default period analysis for Clock 'clk'
Clock period: 4.919ns (frequency: 203.293MHz)
Total number of paths / destination ports: 42 / 14

To the receiver system, it is obtained (after synthesis):

Device utilization summary:

Selected Device : 3s400fg456-4
Number of Slices: 23 out of 3584 0%
Number of Slice Flip Flops: 31 out of 7168 0%
Number of 4 input LUTs: 36 out of 7168 0%
Number of bonded IOBs: 18 out of 264 6%
Number of GCLKs: 1 out of 8 12%
Timing constraint: Default period analysis for Clock 'clk'
Clock period: 4.919ns (frequency: 203.293MHz)
Total number of paths / destination ports: 57 / 29

As can be seen from the two reports, the chip area occupied in a 3s400FG456 FPGA is very small. Therefore, this systems can be integrated on the same chip with others modules.

Besides the high degree of integration, another major advantage is the decrease of computing time over a software solution.

In the Table 1 there are compared the computation time of the hardware system and the estimated response time, when the detection and correction algorithm runs on a computer with a processor which work at 2,8 GHz clock frequency.

Table 1. A comparison between hardware and software processing at transmitter.

k	n	v_t	$T_{hardware}$	$T_{software}$
11	15	0,73	73,785 ns	80,3 ns

To receiver, the computation speed of the system compared with software implementation is higher, because to the hardware system a parallel module is used to correct the error.

Table 2. A comparison between hardware and software processing at receiver

k	n	v_t	$T_{hardware}$	$T_{software}$
11	15	0,73	73,785 ns	107,1 ns

5. Conclusion

The usage of error correcting control is very important in a modern communication system. The BCH codes are being widely used in communication networks, computer networks, satellite communication, magnetic and optical storage systems.

We have presented in this paper the prototyping of a BCH encoder and decoder using a Field Programmable Gate Array (FPGA) reconfigurable chip. We implemented the BCH code in a 3s400FG456 FPGA.

In this implementation we used 15 bits-size word code and the results show that the circuits work quite well. The FPGA implementation of BCH codes leads to a high calculation rate using parallelization. So, we reduce the computation time of control sum at transmission and detection and correction error to receiver.

Our solution can be used for data transmission in real time application. The difference between $T_{hardware}$ and $T_{software}$ increases with the size of word code. A future research direction is to extend our system in order to correct more error bits for larger word code.

6. References

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